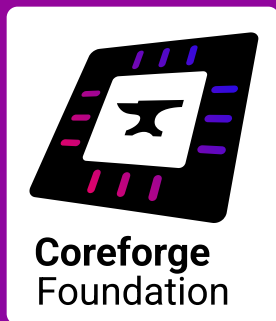


We  
forge  
the  
European  
*open-source*  
RISC-V  
~~processor~~  
future



**Coreblocks**  
our advanced  
RISC-V core

*kuznia-rdzeni.org*

## Coreblocks

### **One of the most parametrisable RISC-V cores**

Many fine tuning possibilities and  
extensive RISC-V support

### **Open-source to the core**

Completely free to use and integrate  
in your products

### **Advanced microarchitecture**

Based on high performance out of order  
microarchitecture for use as an application  
class core

### **Modular and easy to extend**

Ideal for implementing custom instructions,  
accelerators, or conducting research

### **Sovereign design**

Based in Poland, developed fully in Europe

### **Integrations**

Runs mainline Linux, integrates with a system on  
a chip generator

Coreblocks is a unique, well-established project  
with a 4 year history.

Apart from its usage as a FPGA soft core, we aim  
to tape out first ASIC prototypes in the next 2  
years.

Currently we focus on overhauling the internals to  
further improve our processor performance.

Help us deliver the open source processor  
we all need!

## **Support Coreblocks development**

Get in touch [org@kuznia-rdzeni.org](mailto:org@kuznia-rdzeni.org)